ABSTRACT

[0075] A fault tolerant processing circuit comprising at least three processor groupings, a synchronizing circuit and a fault logic circuit. Each of the processor groupings have a plurality of processor grouping inputs and a plurality of processor grouping outputs. The synchronizing circuit comprises a plurality of output synchronizers, wherein each output synchronizer communicates with a corresponding respective processor grouping for synchronizing the output of each processor grouping. A fault logic circuit communicates with the synchronizing circuit. The fault logic circuit comprises a fault detection circuit and a fault mask circuit. The fault logic circuit compares the plurality of processor group outputs to detect errors in any one of the plurality of processor group outputs. An error is detected when none of the at least three processor groups is in a majority of the processor groups. Upon a detected fault, the fault mask circuit masks the output of the respective processor grouping associated with a detected error and signals a detected error. The error signal latch is then used to reset the processor groupings.